

Update on Electronics for mRICH

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Task

- mRICH basic block
- H13700 MCP-PMT with 256 channels
- Compact form-factor: must be able to abut and tile
- Readout close to PMT -> avoid cables and amplification

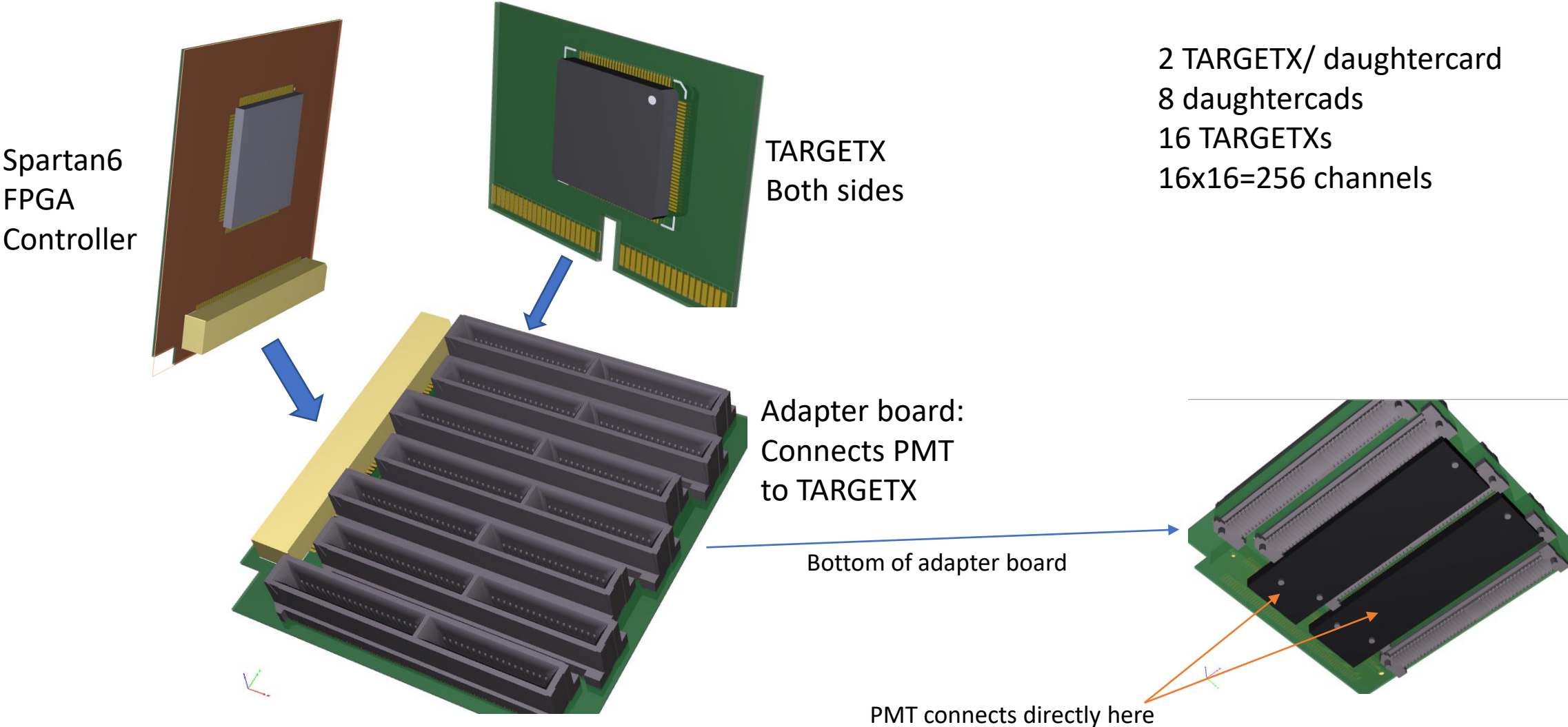
Proposed Solution

- 1st gen mRICH prototype based on existing TARGETX chip:
 - 1GSa/s full waveform sampling
 - 16 us trigger buffer
 - 16 channels
 - Built-in comparator generates trigger primitives
 - Low cost 250nm CMOS
- Used in 3 projects:
 - Belle II KLM upgrade ~20k SiPM channels
 - Borehole Muon Detector (BMD) prototype: ~100 SiPM channels
 - Hawaii Muon Beamline (HMB): ~60 SiPM channels

Benefits and Roadmap

- 1st gen mRICH readout: TARGETX
 - Multiple PCB designs available
 - Variations of firmware available
 - Known testing and calibration procedures
 - Low cost Xilinx Spartan 6 FPGA companion
 - Mechanical design – next slide
- 2nd gen mRICH readout: SiREAD
 - 64 channels
 - 1-3 Gsa/s
 - 2-4 us trigger buffer
 - System-on-Chip
 - Funded commercial grade ASIC through DOE SBIR program
 - Chip fab: Sep 2017, evaluation kits available Jan 2018

Proposed 1st Gen Design

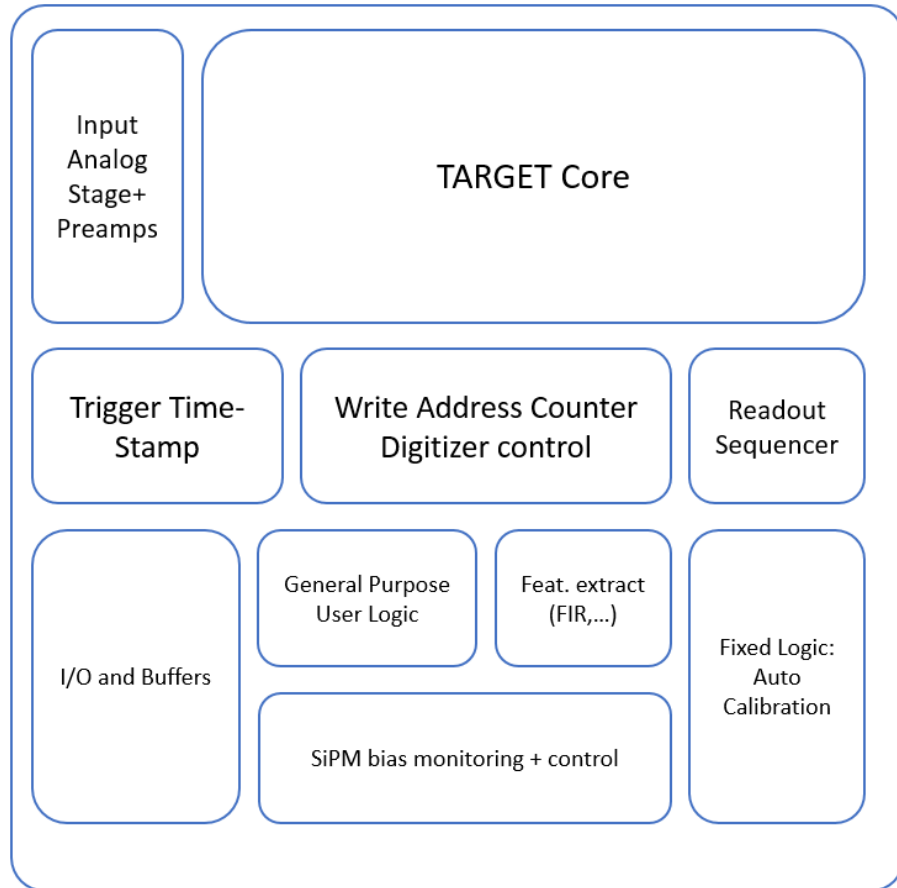


Next steps

- 1st Gen: Allocate formal manpower
 - Finish PCB routing for boards
 - Order parts and fabricate boards
 - Modify existing FPGA firmware
 - Integration and testing
- 2nd Gen: SiREAD based
 - Design and fabricate ASIC as planned
 - Plans for a prototype + mass production

SiREAD: SiPM/PMT Waveform Sampling ASIC

Compact, high performance waveform sampling- current Phase I SBIR



Spec	
Sampling rate	1-3 Gsa/s
ABW	0.8-1.5GHz
Depth	4k Sa
N channels:	64
Fab	250nm CMOS

Key Contribution:

- High performance digitizer: 3+ Gsa/s
- Highly integrated
- Commercially available
- On chip:
 - Analog storage
 - Reconfigurable DSP
 - SiPM Calibration+DACs

Funded and active project- Tape out Sep 2017